Hossen Alyazgi

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Profile & Skills Highlight — Hardware, RTL & Embedded

Low-noise analog and mixed-signal design (op-amp fundamentals, frequency-domain analysis, PCB parasitic mitigation); signal measurement with oscilloscopes, spectrum analyzers, waveform generators and MATLAB automation (ECE 212/316); CMOS transistor-level logic, timing/RC delay, SRAM/DRAM/EEPROM and PCB layout (ECE 334); RTL/FPGA design and verification in Verilog/VHDL/SystemVerilog, UVM, Vivado/Vitis, AXI4; high-speed SerDes (PLLs, CDR, CTLE/DFE, Tx FIR, clock buffering); embedded C/C++ and Python for DSP.

Education

McGill University **Jan. 2026 — present**
M.Eng in Electrical Engineering – Integrated Circuits and Systems Montréal, QC

Relevant Coursework & Practical Knowledge:

- **ECSE 536 RF Microelectronics** – Radio Frequency Integrated Circuits and wireless transceiver architectures. Modelling of passive/active integrated devices. Design of monolithic bipolar and CMOS LNAs, mixers, filters, broadband amplifiers, RF power amplifiers, VCOs, and frequency synthesizers. Analysis of noise and non-linearity in RFICs. RFIC simulation/layout and CAD with Keysight Advanced Design System (ADS).
- **ECSE 527 Optical Engineering** – Designing the optical architecture for a MEMS-based endoscope, utitlizing the Keysight CODE V CAD suite to minimize off-axis aberrations during high-speed raster scanning and validating the integration of micro-optics with electrostatic MEMS actuators.

University of Toronto **Sep. 2019 — Mar. 2025**
B.ASc in Electrical and Computer Engineering Toronto, ON

Professional Experience

Performance & Education Academy **Dec. 2025 — present**
Academic Coach Montréal, QC

- Designing and leading a comprehensive robotics workshop guiding students in building a 3-DOF robotic arm using Technic structural components integrated with an Arduino, servo motors, and ultrasonic sensors for object detection.

Intel Corporation **May 2022 — Sep. 2023**
ASIC Design Engineer Toronto, ON

- Implemented parameterized RTL in **Verilog**/**SystemVerilog** for SerDes PHY modules (CDC logic, PLLs, CDR loops, Tx FIR, power gating, clock buffering)
- Contributed to the development of an adaptive Rx CTLE update engine at 112 Gb/s NRZ & PAM4
- Verified and debugged designs with ModelSim; automated flows using **Perl**, **Bash**, and **Tcl**
- Conducted analog and mixed-signal circuit analysis during verification, examining pin/port behavior, biasing, and signal integrity to validate PLLs, CDR loops, and equalization circuits
- Collaborated with analog design teams to review schematics and identify noise, parasitic, and stability issues impacting SerDes front-end performance

Projects

NeuroScope — McGill University TechAccel Venture **Jan. 2026 — present**
Lead R&D Engineer Montréal, QC

- Developing a high-sensitivity optical acquisition system implementing real-time synchronous demodulation (lock-in amplification) to optimize signal fidelity using Ansys Lumerical.
- Selected for the McGill TechAccel program to advance a proprietary optoelectronic platform, leading validation of a custom PCB architecture using Altium Designer for low-latency neural recording.

FPGA Hardware Synthesizer Capstone — University of Toronto **Sep. 2023 — May 2024**
Principal Design Engineer Toronto, ON

- Designed a real-time pitch-analysis engine (FFT) on Digilent Nexys Video Artix-7 with custom **VHDL**
- Integrated MIG7 DDR3 and low-speed I/O (UART, SPI, I2C, I2S); automated Vivado flow with **Tcl and Bash**. Data pre-processing and pipelining done through **Python**
- Instantiated MicroBlaze soft-CPU with AXI4 interconnect; wrote bare-metal DSP firmware in **C (Vitis SDK)** with DMA acceleration